

Modelling of Organic Field-Effect Transistors for Technology and Circuit Design

S. Mijalković, D. Green, A. Nejm, G. Whiting, A. Rankov, E. Smith, J. Halls and C. Murphy

Abstract— As organic field-effect transistors (OFETs) are preparing to take a key role in the flexible and low cost electronics applications, there is a pressing need for predictive device models to support technology optimization and circuit design. This paper focuses on the specific OFET features that challenge current modelling approaches. The presented modelling techniques range from the fundamental semiconductor equations to compact device model representations as required for implementation in advanced TCAD and EDA commercial tools. The models are verified with measured characteristics of advanced OFET device structures.

I. INTRODUCTION

Organic semiconductors (OSC) combine in a unique way the electrical properties of semiconductors with the properties typical of plastics, such as easy fabrication, mechanical flexibility, and low cost. The rapid development of the field of organic electronics is mainly driven by attractive applications that would exploit the plastic-like features of the organic semiconductors. Some of the desired future applications include: e-paper, e-skin, e-nose, smart windows and perhaps molecular computers. More realistic for the near future are applications in RFID tags, analytical sensors and active matrix displays [1]. The first full-colour, flexible and all OSC displays have been recently reported by the industry.

Organic field-effect transistors (OFETs) form the basis of organic electronic circuits. To be successful, OFETs have to achieve a performance comparable to that of currently used inorganic thin film transistors (TFTs) at significantly lower production price. Due to the considerable advances in terms of material and device fabrication during the last decade, the performance of OFETs is approaching that of amorphous silicon (a-Si) TFTs. But, this performance is still quite a long way behind other inorganic counterparts. A lot of work is yet to be done in improving the electrical characteristics, reliability and uniformity at the process, device and circuit design levels.

The inorganic semiconductor industry relies extensively on electronic design automation (EDA) tools to

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support the iterative cycles of process, device and circuit technology improvements. In the inorganic electronic industry EDA has raised the designer productivity by a factor of more than a thousand in the last quarter of a century [2]. These EDA tools could be equally important in increasing the development rate of the OFET technology, speeding up its movement from the laboratory to the shop floor. However, EDA has not yet become a common practice in organic electronic technology and circuit design. EDA tools essentially depend on numerical and analytical process and device models which are, in the case of OFETs, not yet matured and quite sparsely implemented in commercial EDA tools.

OFET models are required on two different design levels. The optimization of the device geometry and technology require fundamental numerical multi-dimensional models governing the charge distribution and carrier transport in the organic semiconductors. On the other hand, efficient and accurate compact, analytical device models are required to provide a bridge between the OFET technology and the circuit design. This paper focuses on some critical issues of both modelling areas. The presented modelling approaches are implemented in the latest generation of commercial EDA tools and verified with measurement data obtained from the advanced OFET structures and technology.

This paper is organized as follows. Section II provides an overview of the explored OFET architectures and the main processing steps used to fabricate the test samples. OFET specific modelling challenges are discussed in Section III. Section IV presents the essential modelling extensions required for OFET technology design and model verification with measured OFET characteristics. The circuit design oriented compact modelling methodology and comparison with measured OFET characteristics is presented in Section V.

II. OFET TEST STRUCTURES

A. Device Architectures

OFETs can be fabricated in four possible device architectures depending on the relative position of the source/drain and gate contacts with respect to the OSC layer [3]. The possible architectures include the well known top-gate-top-contact structure, typical for standard silicon MOSFETs, as well as bottom-gate-bottom-contact structure, commonly used by inorganic

TFTs. However, OTFT can be realized in the top-gate-bottom-contacts and bottom-gate-top-contact architectures as well.

The two OFET architectures that have been considered here are the top-gate-bottom-contact (TGBC) structure, shown in Fig. 1 and used for the verification of the technology design models, and bottom-gate-bottom-contact (BGBC) structure, shown in Fig. 2, whose measured characteristics have been used to extract the OFET compact model parameters.

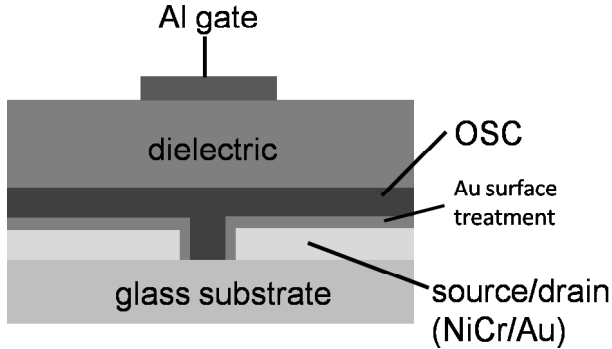


Fig. 1. Top gate bottom contact (TGBC) OTFT device architecture

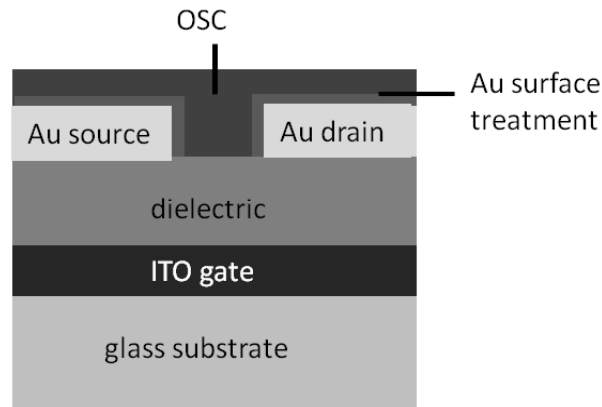


Fig. 2. Bottom gate bottom contact (BGBC) OTFT device architecture

The TGBC architecture has in principle a larger injection area and thus a lower contact resistance which enables higher currents for the same applied voltages in comparison to the BGBC structure. It is an easier to manufacture structure since source/drain contacts are patterned on a substrate rather than on a dielectric or OSC layer. However, this structure has limitations because of lack of suitable dielectric materials.

On the other hand, the BGBC architecture has been more often used in OFET research. A wider range of potential solution processable dielectrics can be used

with BGBC architecture to provide a smooth dielectric/OSC interface. However, the downside of this device structure is a high contact resistance due to the low area for charge injection and extraction.

B. Processing

The test structures with the TGBC OFET architecture were fabricated starting with the evaporation of gold source-drain contacts onto the glass substrate. In order to ensure good energy level matching between Au and OSC bands, a proprietary self-assembled monolayer (SAM) was spin-coated onto the substrates. A solvent spin-rinse was applied to ensure local adhesion of the SAM to the source-drain coated areas of the substrate. It was followed by a spin coating of OSC onto the surface. Dielectric was then spin coated over the OSC and finally a gate (Au or Al) was evaporated.

The preparation of the BGBC test OFET structures started with the indium tin oxide (ITO) coated glass substrates. They are patterned photo-lithographically to produce the gate contacts. A proprietary dielectric polymer was then spin-coated onto the surface. The substrate was then annealed, under a nitrogen atmosphere, to cross-link the dielectric film. Gold (Au) was then thermally evaporated through a shadow mask to produce the source/drain contacts. Finally, following a SAM treatment the proprietary OSC was spin-coated.

A range of devices with different geometries were fabricated in both architectures. The test devices were encapsulated with a glass, containing an adhesive desiccant, using a UV curable epoxy to adhere the can to the substrate. The completed devices were then removed from the nitrogen environment, scribed and broken into smaller (25 mm) cells and tested using an HP/Agilent 4156B precision semiconductor parameter analyser with contact made using Au-coated, spring-loaded pins.

III. OFET MODELLING CHALLENGES

A range of peculiar features in the OFET device properties, electro-static behavior and carrier transport require special consideration and different modelling approaches than their inorganic counterparts.

OFETs are typically realized using an undoped OSC. The dopants in inorganic semiconductors are essentially maintaining equilibrium carrier concentration and conductivity. On the other hand, the carriers that contribute to the charge distribution and transport in OFETs must be injected from the metallic contacts. The injected carriers can occupy the states in semiconductors HOMO and LUMO bands but also the localized states in the band-gap which are induced by defects and unwanted impurities.

The free carrier concentration is typically negligible compared to the trapped carrier concentration and the latter is dominant in defining the charge and electric field distribution. Due to this fact, it is required to

reformulate the carrier concentration dependencies on the Fermi and electrical potential in both technology and circuit design models.

Without dopants and a particular semiconductor type, OFETs can operate in the electron or hole carrier accumulation modes depending on the polarity of the gate voltage [4], [5]. The energy barrier at the contacts often provides only injection of a single carrier type (electrons or holes) and OFETs typically operate in a unipolar accumulation mode (as an effective NMOS or PMOS device).

The source and drain contacts have no junction isolation typical for inorganic MOSFETs. Consequently, a drain/source leakage current is limited by the intrinsic carrier occupancy of the localized and band states rather than reverse junction current. For higher leakage current levels, the depletion operation mode can be also of interest for an accurate compact OFET modelling.

In OFETs only the free carriers in the bands and the carriers in the shallow traps close to the bands participate in the carrier transport. In OFETs models, the concentration of mobile carriers should be separated from the total injected carrier concentration. But, it is also common to assume that all carriers participate in the transport equations with an effective carrier mobility.

OFETs are typically characterized with much lower carrier mobility than inorganic MOSFETs [6]. The mobility is also gate voltage dependent in the similar way as in a-Si TFTs. A small carrier mobility in OTFTs is usually attributed to the weak intermolecular interaction in the solid material state, impurities and defects as well as an inefficient injection/extraction capability of carriers at the metal contacts [7]. The voltage dependence is usually explained in the following way: as more charges are injected with the increase of gate voltage, more traps will be filled reducing the trapping rate and thus increasing the mobility of carriers.

Another parameter that dominates the performance of OFETs is contact resistance [8]. Ideally, it should be ohmic and small in order to enable that the whole voltage applied to the device contributes to the transport current. However, typically in case of OFETs, these contacts are either high value ohmic or non-ohmic (Schottky) and considerably affect the device transport current [9].

IV. TECHNOLOGY DESIGN MODELLING

Technology design device models (also known as TCAD device models) are based on the numerical solution of the coupled Poisson and carrier transport equations. In order to be useful for OTFTs, the standard drift-diffusion carrier transport equations should be enhanced by appropriate models for the carrier concentration and mobility. The model description is based on a unipolar electron transport but it is straightforward to

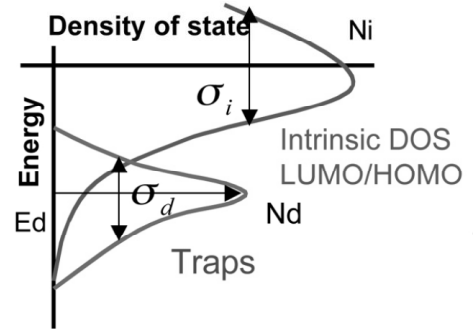


Fig. 3. Simplified graphical representation of the double peak Gaussian DOS distribution used within the presented simulations

extend it to the case of bipolar carrier transport.

A. Carrier Concentration

The electron concentration is obtained from [10]

$$n = \int_{-\infty}^{\infty} g(E) f_{\text{HSR}}(E, n) dE \quad (1)$$

where $g(E)$ is the density of states (DOS) energy profile and $f_{\text{HSR}}(E, n)$ is the Hall-Shockley-Read (HSR) distribution function. HSR distribution function gives the probability of the state occupation in terms of the energy E and the electron concentration n . In equilibrium, $f_{\text{HSR}}(E, n)$ is identical to the standard Fermi-Dirac statistical distribution.

The DOS profile $g(E)$ is based on a double peak Gaussian distribution [10], [11]:

$$g(E) = \frac{N_i}{\sigma_i} f\left(\frac{E - E_c}{\sigma_i}\right) + \frac{N_d}{\sigma_d} f\left(\frac{E - E_c + E_d}{\sigma_d}\right) \quad (2)$$

where

$$f(x) = \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{x^2}{2}\right) \quad (3)$$

is the density function of the standard normal distribution, E_c is the bottom energy level of the conduction band, N_i and N_d are the total intrinsic and trap densities, σ_i and σ_d are the corresponding Gaussian widths while E_d represents the energy shift between the intrinsic and trap states. A simplified graphical representation of the double peak Gaussian distribution of the DOS is shown in Fig. 3.

B. Carrier Mobility

The charge transport occurs in OSC dominantly via the hopping of carriers between localized states. The field independent hopping mobility is calculated from [11]:

$$\mu_0 = \frac{qv_0}{kT} n_t^{-2/3} \exp\left[-2\kappa \left(\frac{3\chi}{4\pi n_t}\right)^{1/3}\right] \quad (4)$$

where v_0 is the attempt-to-jump frequency, χ is the percolation constant, κ is the reciprocal of the carrier localization radius and

$$n_t = \int_{-\infty}^{E_{tn}} g(E) dE \quad (5)$$

where E_{tn} is the effective transport energy for the electrons.

It is typically considered that charge transport will become field dependent in organic materials at high electric fields ($\approx 10^5$ V/cm). This phenomenon is described through a Poole-Frenkel mechanism. Field dependent mobility effects were also included within the simulations. The Poole-Frenkel field dependent mobility model used in the simulations is described by [12], [13]:

$$\mu_{PF}(E) = \mu_0 \cdot \exp \left[-\frac{\Delta}{kT_0} + \frac{\delta}{kT_0} \sqrt{F} \right] \quad (6)$$

where μ_0 is the low field mobility, Δ is the activation energy, F is the electric field intensity and

$$\delta = \sqrt{\frac{q}{\pi\epsilon_s}} \quad (7)$$

is the Poole-Frenkel Factor where ϵ_s is the permittivity of the semiconductor.

C. TGBC Case Study

Two-dimensional physical modelling of the experimental structure has been undertaken. The simulated structure is shown in Fig. 4. It was created by Silvaco's Athena [14], which is a physics based two-dimensional process simulator. The dimensions of the simulated structure, which include conformal layers of OSC, oxide and Al gate, were the same as the experimental dimensions. The organic material defined within the simulations was based on parameters and values physically extracted from the measured device.

The following figures present and compare simulated results obtained by the Silvaco's device simulator Atlas [15] and measured input and output TGBC OFET test device characteristics at room temperature. Two different gate biases are considered to ensure that the model can represent the measured results at both high and low current levels. Besides using DOS, Hopping and Poole-Frenkel mobility models, the Langevin Recombination model [16] has been also employed as well as the effect of series resistance and interfacial charge between the oxide and OSC layer.

Shown in Fig. 5 are input characteristics with a drain bias of -3 V. The threshold voltage was found to be sensitive to the interfacial charge between the oxide and the OSC. The simulation results show a linear increase in current, unlike the measured results, which

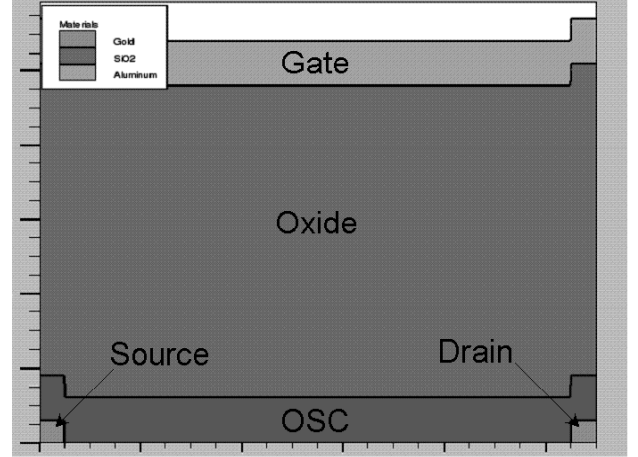


Fig. 4. Simulated Organic TFT structure with conformal OSC layer (note that the curvature in the OSC, oxide and contacts is not clearly visible due to distortions in scale).

are sub-linear at high gate bias. This characteristic is commonly attributed to the effects of contact resistance. Although contact resistance has been included in the physical model, the magnitude currently considered has no noticeable effect on the input characteristics. For the input characteristics, the mean percentage error currently achieved is in the region of 19%.

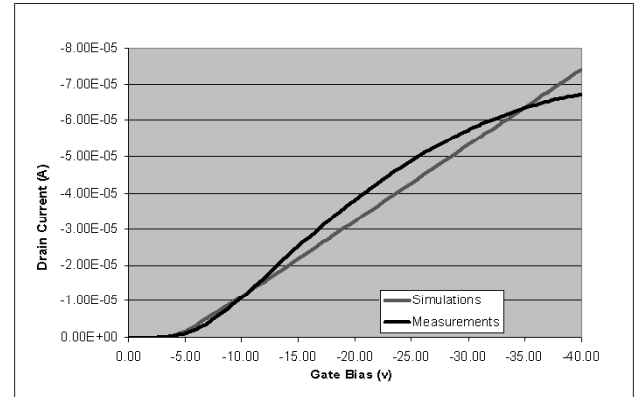


Fig. 5. Comparison between simulated and measured transfer characteristics ($V_d = -3$ V). The threshold voltage can be accurately modelled through interface charge control. Simulation results show a monotonic increase in current due to a negligible effect from contact resistance.

Shown in Fig. 6 are output characteristics at a gate bias of -10 V from simulations and measurements. In this instances a highly accurate fit is achieved in the linear region ($< 2\%$). Considering the current range of measured results the error of $< 15\%$ achieved in the saturation region is considered as acceptable. Overall a mean percentage error of 14.4% has been achieved.

Shown in Fig. 7 are output characteristics at a gate bias of -30 V. The measured results clearly indicate some form of leakage through the gate contact. It has

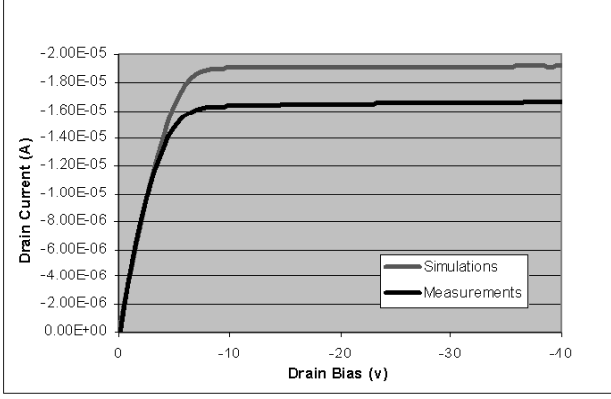


Fig. 6. Comparison between simulated and measured output characteristics ($V_g = -10$ V). A highly accurate fit in the linear region (2 % error) is achieved. Simulations overestimate the current in the saturation regime giving an error of 15%

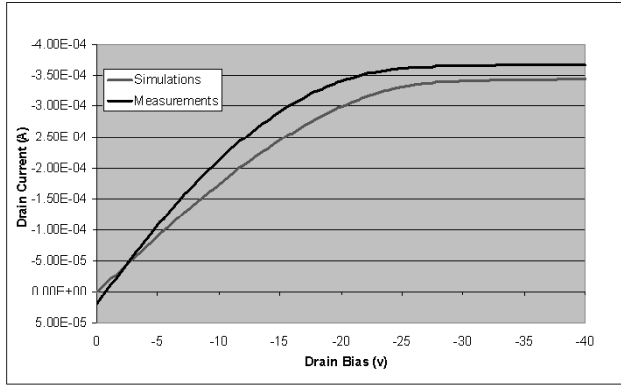


Fig. 7. Comparison between simulated and measured output characteristics ($V_g = -30$ V). Measured results indicate a leakage current through the gate contact, which is not accounted for in simulations. Consequently an error of 17 % is achieved.

recently been found that this is due to the devices being unpatterned and can therefore not be considered as a characteristic of the device or oxide layer itself. As this leakage current has not been included in the physical model an error in the linear regime of $< 18\%$ is achieved and in the saturation regime an error of $< 7\%$ is achieved. The mean percentage error in this instance is $< 17\%$. It is believed that this could be reduced to approximately 10% if the additional leakage current that is observed was addressed.

V. CIRCUIT DESIGN MODELLING

The standard compact models for inorganic MOSFETs only consider the depletion/inversion device operation mode [17], which is not suitable for the accumulation operation mode of OFETs. Some of the models that account for the accumulation operation mode [18] are oriented towards particular applications and not widely available in EDA tools. The closest to serve as

potential compact OTFT models are some of the inorganic TFT models [19] based on quite generic threshold voltage empirical descriptions of the transfer current.

The main goal of this section is to present the essential ingredients of a new physical surface-potential based OFET compact model. The performance of the model is verified in the BGBC case study.

A. Carrier Concentration

In most practical cases, the acceptor like DOS can be approximated by the exponential distribution

$$g(E) = \frac{N_A}{kT_0} \exp\left(\frac{E - E_c}{kT_0}\right) \quad (8)$$

where N_A is the total density and T_0 is a characteristic temperature that indicates the width of the exponential DOS distribution.

Assuming a slowly varying DOS distribution $g(E)$ ($T \ll T_0$) and the zero Kelvin approximation of the Fermi-Dirac distribution, the electron concentration is obtained as

$$n = \int_{-\infty}^{E_{fn}} g(E) dE = N_A \exp\left(\frac{E_{fn} - E_c}{kT_0}\right) \quad (9)$$

where E_{fn} is a quasi-Fermi energy. The electron concentration can be also expressed in terms of electrical and Fermi potentials, ψ and ϕ_n , as

$$n = n_0 \exp\left(\frac{\psi - \phi_n}{V_{T0}}\right) \quad (10)$$

where n_0 is the intrinsic electron concentration and $V_{T0} = kT_0/q$ is the effective thermal voltage.

B. Surface Potential Equation

Neglecting the variation of the electric field along the gate-insulator and OSC interface (gradual channel approximation) and integrating the Poisson equation from the equilibrium point, where $n = n_0$, to the interface, the total semiconductor sheet charge per unit area Q'_C can be expressed in terms of the surface potential ψ_s as

$$-Q'_C = \text{sign}(\psi_s - \phi_n) \sqrt{2q\epsilon_s n_0 V_{T0}} \cdot h\left(\frac{\psi_s - \phi_n}{V_{T0}}\right) \quad (11)$$

where ϵ_s is the permittivity of the semiconductor and $h(x)$ is a non-negative function

$$h(x) = \exp(x) - x - 1. \quad (12)$$

The surface potential ψ_s is only implicitly available from the charge equilibrium equation

$$Q'_G + Q'_C = 0 \quad (13)$$

where

$$Q'_G = C'_i (V_G - V_{FB} - \psi_s) \quad (14)$$

is the gate charge per unit area. Here C'_i is the gate insulator capacitance per unit area, V_G is the applied gate voltage, while V_{FB} is the flat-band voltage that accounts for the bias independent space charge present in the gate-insulator.

The surface potential equation (13) can be also expressed as

$$(V_G - V_{FB} - \psi_s)^2 = V_{T0} \gamma^2 \cdot g \left(\frac{\psi_s - \phi_n}{V_{T0}} \right) \quad (15)$$

where

$$\gamma = \frac{\sqrt{2q\epsilon_s n_0}}{C'_i} \quad (16)$$

is the body factor. There is no a closed form analytical solution for the surface potential equation (15) but very accurate analytical approximations have been proposed [20].

C. Transport Current

Assuming a laminar current flow parallel to the gate-insulator and OSC interface, and neglecting the carrier recombination, the intrinsic transport currents can be represented in the integral form as [17]

$$I_T = \frac{W}{L} \int_{V'_s}^{V'_D} G'_C d\phi_n \quad (17)$$

where G'_C is the semiconductor sheet conductivity, W and L are the effective transistor width and length, while V'_s and V'_D are intrinsic source and drain biases.

In the accumulation operation mode ($\psi_s > \phi_n$), the sheet conductance is defined as

$$G'_C = G_{C0} + \mu'_n (-Q'_C) \quad (18)$$

where G_{C0} is the sheet semiconductor conductivity at the flat band biasing condition and $\mu'_n > 0$ is the effective mobility for the accumulated sheet electron charge.

Following the ideas of the percolation model for variable range hopping [21], [22], the effective mobility of the accumulated sheet electron charge is introduced here as

$$\mu'_n = \alpha (-Q'_C)^\beta \quad (19)$$

where the model parameters α and β control the influence of the accumulated electron charge on the mobility. For moderate and strong accumulation, the percolation theory predicts

$$\beta = 2 \left(\frac{T_0}{T} - 1 \right) \quad (20)$$

but to release the correlation constraints among the parameters, β has been introduced as a separate temperature dependent model parameter.

The transport current is split into two components as

$$I_T = I_{T0} + I_{TC} \quad (21)$$

where

$$I_{T0} = \frac{W}{L} G_{C0} (V'_D - V'_s) \quad (22)$$

and

$$I_{TC} = \alpha \frac{W}{L} \int_{V'_s}^{V'_D} (-Q'_C)^{\beta+1} d\phi_n. \quad (23)$$

Here, I_{T0} is the gate bias independent leakage current while I_{TC} defines the transport current increase due to the carrier accumulation.

Introducing the change of variables

$$d\phi_n = \frac{d\phi_n}{d\psi_s} d\psi_s = \left(1 - \frac{2V_{T0}C'_i}{Q'_C} \right) \frac{dQ'_C}{C'_i}, \quad (24)$$

obtained from the surface potential equation as a good approximation in the moderate and strong accumulation operation mode, (23) can be explicitly expressed in terms of the sheet charge Q'_C at the source and drain side as

$$I_{TC} = I_{TC}^{\text{drift}} + I_{TC}^{\text{diff}} \quad (25)$$

where

$$I_{TC}^{\text{drift}} = \alpha \frac{W}{L} \left[\frac{(-Q'_C)_S^{\beta+2} - (-Q'_C)_D^{\beta+2}}{(\beta+2)C'_i} \right] \quad (26)$$

and

$$I_{TC}^{\text{diff}} = 2\alpha V_{T0} \frac{W}{L} \left[\frac{(-Q'_C)_S^{\beta+1} - (-Q'_C)_D^{\beta+1}}{(\beta+1)} \right] \quad (27)$$

are the drift and diffusion components of I_{TC} .

D. Equivalent Circuit

In the model equivalent circuit, shown in Fig. 8, the transfer current is introduced as a voltage controlled current source. The intrinsic model has been extended by the source and drain contact resistances R_S and R_D connecting the intrinsic source and drain nodes, S' and D' , to the corresponding externally available source and drain nodes, S and D .

The gate-source and gate-drain charges, Q_{GS} and Q_{GD} , as well as the gate-source and gate-drain tunneling currents, I_{GS} and I_{GD} , are implemented using the common surface potential based modelling approach [17].

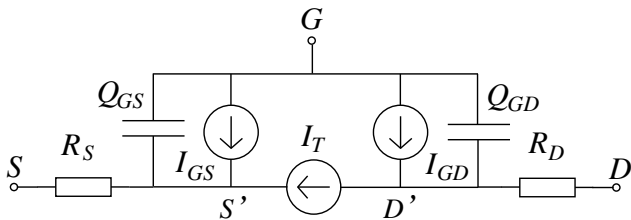


Fig. 8. Equivalent circuit

E. BGBC Case Study

The governing compact modelling equations are implemented in the Verilog-A language and simulated by the circuit simulator SmartSpice [23] equipped with a Verilog-A compiler. The measured characteristics of the BGBC test devices have been used to extract the model parameters using the extraction tool Utmost IV [24] that interactively employs the SmartSpice simulator during the parameter optimization procedure.

The resulting simulated input characteristics in linear region and saturation regions are compared to the measured the BGBC test structure characteristics in Fig. 9. Fig. 10 shows the comparison of measured and simulated BGBC test structure output characteristics.

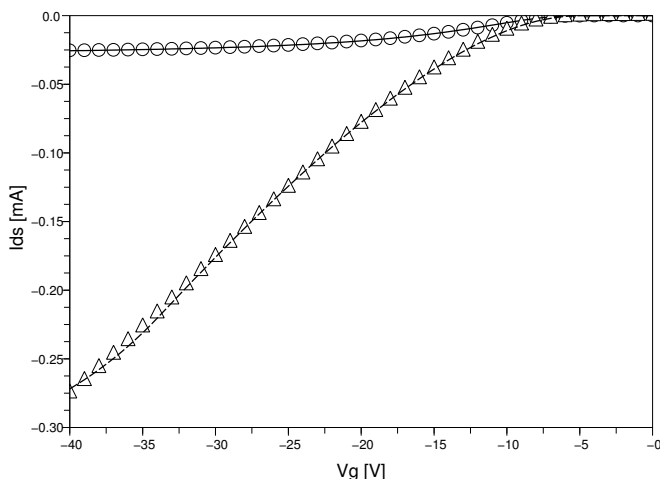


Fig. 9. Comparison between simulated (lines) and measured (symbols) input characteristics of the BGBC test OTFT. The full line and circles annotate linear operation region with $V_{ds} = -3$ V while dashed line and triangles correspond to the saturation operation region with $V_{ds} = -30$ V.

The model has demonstrated a capability to fit the measured OFET input and output characteristics over a wide range of device biases. However, because of the variability in the measurement data due to charge trap memory effects, the parameter extraction has been performed separately for each characteristics. One possible solution to overcoming this problem is to extract parameters simultaneously for several properly selected characteristics.

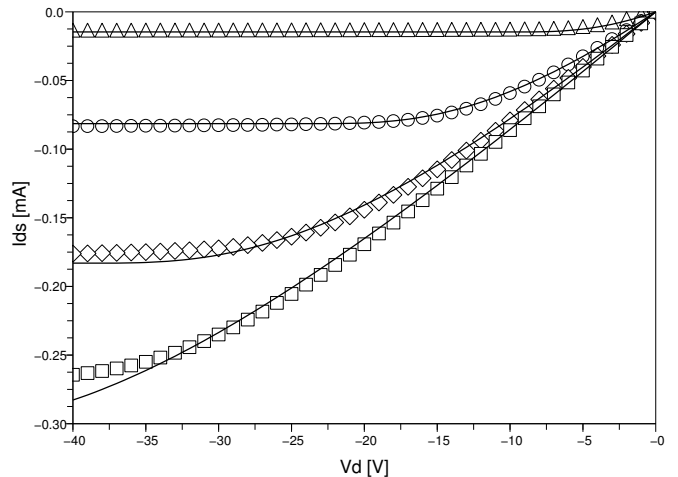


Fig. 10. Comparison between simulated (lines) and measured (symbols) output characteristics of BGBC test OFET. The squares annotate $V_g = -40$ V, diamonds $V_g = -30$ V, circles $V_g = -20$ V and triangles $V_g = -10$ V.

VI. CONCLUSIONS

EDA tools equipped with accurate physical OFET models are essential to speed up the optimization of device performance and to provide a bridge towards the organic circuit design.

It is demonstrated that applying advanced OSC charge transport and mobility models in the multi-dimensional device simulator Atlas can enable the accurate physical modelling of OFET devices. The relative error between simulated and measured results is typically $< 15\%$. It is considered that at this stage this is an acceptable level due to the current spread of measured results. With further investigation into modelling the DOS, carrier mobility, contact phenomena and the gate tunneling current, it is expected that the error between measured and simulated results can be reduced further. Once the physical model is further advanced it is foreseen that investigations into the effect of temperature and long term electrical stressing will also be undertaken through numerical device simulations.

Following the best modelling practices from the inorganic world, the concept of surface potential has been extended here to create a new physical OFET compact model. It also represents a basis for a physical charge control model to support dynamic device operation. It is demonstrated that the intrinsic transport current model can provide very good fit of the measured test BGBC OFET input and output characteristics. The model can be further extended to account for: the bias dependent contact resistances, gate tunneling current and effects of interface trap states. Perhaps the biggest challenge will be handling OTFT memory effects (bias stress instability and hysteresis) within the model and the corresponding circuit design.

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